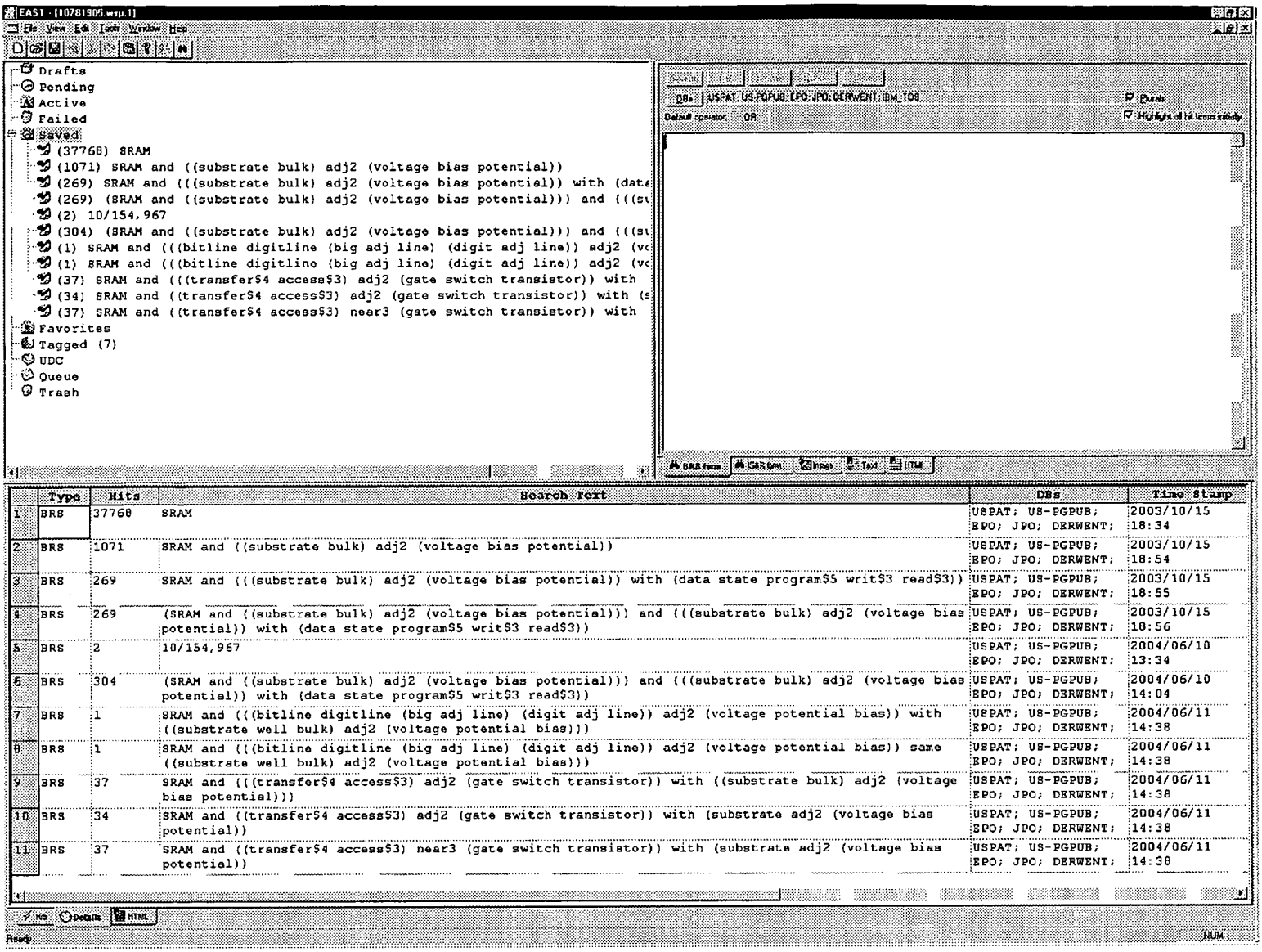

	Type	Hits	Search Text	DBs	Time Stamp
1	BRS	37768	SRAM	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2003/10/15 18:34
2	BRS	1071	SRAM and ((substrate bulk) adj2 (voltage bias potential))	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2003/10/15 18:54
3	BRS	269	SRAM and (((substrate bulk) adj2 (voltage bias potential)) with (data state program$5 writ$3 read$3))	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2003/10/15 18:55
4	BRS	269	(SRAM and ((substrate bulk) adj2 (voltage bias potential))) and (((substrate bulk) adj2 (voltage bias potential)) with (data state program$5 writ$3 read$3))	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2003/10/15 18:56
5	BRS	2	10/154,967	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2004/06/10 13:34
6	BRS	304	(SRAM and ((substrate bulk) adj2 (voltage bias potential))) and (((substrate bulk) adj2 (voltage bias potential)) with (data state program$5 writ$3 read$3))	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2004/06/10 14:04
7	BRS	1	SRAM and (((bitline digitline (big adj line) (digit adj line)) adj2 (voltage potential bias)) with ((substrate well bulk) adj2 (voltage potential bias)))	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2004/06/11 14:38
8	BRS	1	SRAM and (((bitline digitline (big adj line) (digit adj line)) adj2 (voltage potential bias)) same ((substrate well bulk) adj2 (voltage potential bias)))	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2004/06/11 14:38
9	BRS	37	SRAM and (((transfer$4 access$3) adj2 (gate switch transistor)) with ((substrate bulk) adj2 (voltage bias potential)))	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2004/06/11 14:38
10	BRS	34	SRAM and ((transfer$4 access$3) adj2 (gate switch transistor)) with (substrate adj2 (voltage bias potential))	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2004/06/11 14:38
11	BRS	37	SRAM and ((transfer$4 access$3) near3 (gate switch transistor)) with (substrate adj2 (voltage bias potential))	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2004/06/11 14:38